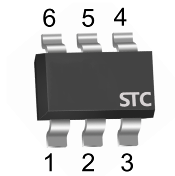
1.2MHZ, 28V OUTPUT, 2A BOOST REGULATOR

FEATURES

- Wide Operating Input Voltage: 2V ~ 24V
- Up to 28V Output Voltage
- Fixed 1.2MHz Switching Frequency
- Integrated 80mΩ Power MOSFET
- Internal 4A Switch Current Limit
- Integrated Internal Compensation
- Output Adjustable from 0.6V
- Thermal Shutdown
- Available in a SOT-23-6L Package



SOT-23-6L

DESCRIPTION

The ***STComponet*** ST3710 is a constant frequency, current mode step-up converter intended for small, low power applications. The ST3710 switches at 1.2MHz and allows the use of tiny, low cost capacitors and inductors 2mm or less in height. Internal soft-start results in small inrush current and extends battery life.

The ST3710 includes under-voltage lockout, current limiting, and thermal overload protection to prevent damage in the event of an output overload. The ST3710 is available in a small SOT-23-6L package.

DEVICE SUMMARY

Ordering Code	Package Material	Package Type	Marking [1]	Shipping
ST3710M	Lead Free	SOT-23-6L	KCYLL	Taping reel
ST3710MG	Halogen Free			Taping reel

Note 1: **KC**: Specific device code. **Y**: Year code; **LL**: Lot number code.

TYPICAL APPLICATION CIRCUIT

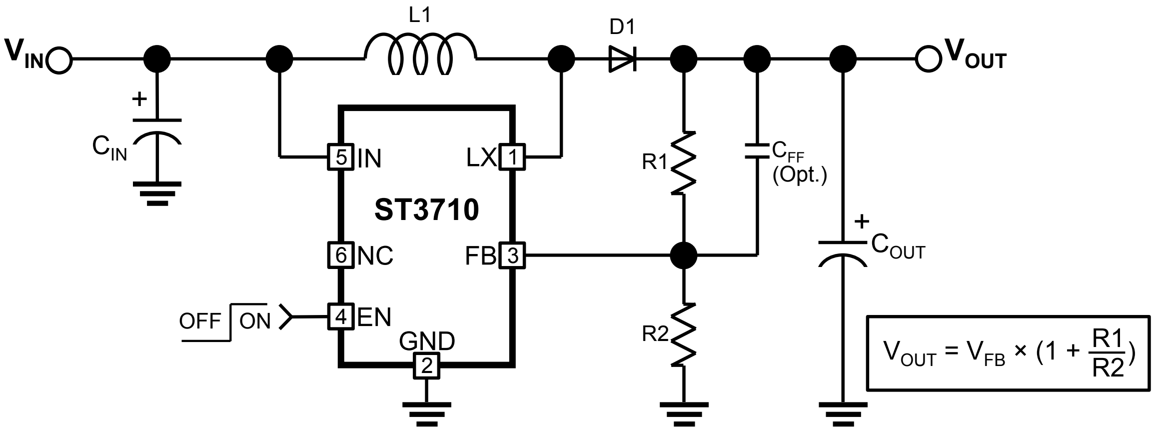


Figure 1: ST3710 Basic Application Circuit

PIN DESCRIPTION

Pin No.	Pin Name	Function Description
1	LX	**Power Switch Output.** LX is the drain of the internal MOSFET switch. Connect the power inductor and rectifier to LX. LX can swing between GND and 28V.
2	GND	**Ground Terminal.**
3	FB	**Adjustable Version Feedback Pin.** The FB voltage is 0.6V. Connect a resistor divider to FB.
4	EN	**Chip Enable Pin.** A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input supply for automatic startup.
5	IN	**Power Supply Input Terminal.** Must be locally bypassed.
6	NC	Not connection.

INTERNAL SCHEMATIC DIAGRAM

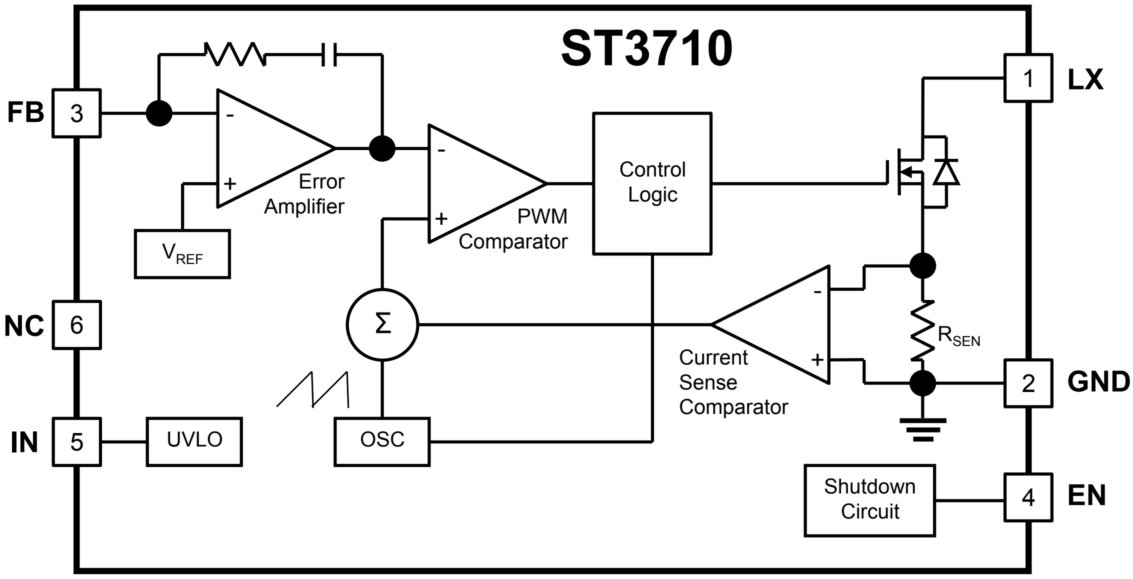


Figure 2: ST3710 Block Diagram

ABSOLUTE MAXIMUM RATINGS [2]

T_A = 25°C, All voltage respect to GND unless otherwise specified.

PARAMETER		SYMBOL	RATINGS	UNIT
IN & EN Pins Input Voltage		V_{IN}, V_{EN}	-0.3 ~ +26	V
LX Pin Voltage		V_{LX}	-0.3 ~ +30	V
FB Pin Voltage		V_{FB}	-0.3 ~ +6.0	V
Continuous Power Dissipation		P_D	500	mW
Thermal Resistance	Junction-to-Ambient	$R_{\theta JA}$	250	°C/W
	Junction-to-Case	$R_{\theta JC}$	130	°C/W
Maximum Junction Temperature		T_{JMAX}	+150	°C
Operating Free Air Temperature Range		T_A	-40 ~ +85	°C
Storage Temperature		T_{stg}	-65 ~ +150	°C
Soldering Temperature & Time (10 Seconds)		T_{solder}	+260	°C

Note 2: Absolute Maximum Ratings are those values beyond which the device could be permanently damaged. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

T_A = 25°C, All voltage respect to GND unless otherwise specified.

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Input Voltage	V_{IN}	2 ~ 24	V
Output Voltage	V_{OUT}	V_{IN} ~ 28	V
Operating Junction Temperature Range	T_J	-40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C, All voltage respect to GND unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Shutdown Current	I_{SHDN}	V_{EN} = 0V		0.1	1	μA
PFM Mode Quiescent Current	I_{CC1}	V_{FB} = 0.7V, no switch		50	100	μA
PWM Mode Quiescent Current	I_{CC2}	V_{FB} = 0.5V, switch		0.2	0.4	mA
LX Pin Leakage Current	I_{LX}	V_{LX} = 20V			1	μA
LX On-Resistance	R_{ON}			80	150	mΩ
Operating Input Voltage	V_{IN}		2		24	V
Internal MOSFET Current Limit(3)	I_{LMT}	V_{IN} = 5V, duty cycle = 50%	3			A
Oscillator Frequency	f_{OSC}	V_{FB} = 0.75V		1.2		MHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.7V		90		%
Feedback Voltage	V_{FB}		588	600	612	mV
FB Input Bias Current	I_{FB}	V_{FB} = 0.6V	-50	-10		nA
EN Threshold	V_{EN}			1		V
Thermal Shutdown(4)	T_{SD}			160		°C

Note 3: MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.
Note 4: Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

BASIC OPERATION

The ST3710 uses a fixed frequency, peak current mode boost regulator architecture to regulate voltage at the feedback pin. The operation of the ST3710 can be understood by referring to the block diagram of *Figure 2*. At the start of each oscillator cycle the MOSFET is turned on through the control circuitry. To prevent sub-harmonic oscillations at duty cycles greater than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the negative input of the PWM comparator. When this voltage equals the output voltage of the error amplifier the power MOSFET is turned off. The voltage at the output of the error amplifier is an amplified version of the difference between the 0.6V band gap reference voltage and the feedback voltage. In this way the peak current level keeps the output in regulation. If the feedback voltage starts to drop, the output of the error amplifier increases. These results in more current to flow through the power MOSFET, thus increasing the power delivered to the output. The ST3710 has internal soft start to limit the amount of input current at startup and to also limit the amount of overshoot on the output.

APPLICATIONS INFORMATION

Setting the Output Voltage

ST3710 are internally compensated and do not require external components to achieve stable operation. *Figure 1* shows the basic application circuit of ST3710. The external resistor sets the output voltage according to following equation:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

Inductor Selection

The ST3710 boost converter can utilize small surface mount and chip inductors due to the fast 1.2MHz switching frequency. Inductor values between 2.2μH and 10μH are suitable for most applications. Larger values of inductance will allow slightly greater output current capability by reducing the inductor ripple current. Increasing the inductance above 10μH will increase size while providing little improvement in output current capability. The minimum boost inductance value is giving by:

$$L > \frac{V_{IN} \times (V_{OUT} + V_{DIODE} - V_{IN})}{f_{OSC} \times I_{RIPPLE} \times (Vout + V_{DIODE})}$$

Where I_{RIPPLE}: Peak-to-peak inductor current

V_{IN}: Input voltage

V_{OUT}: Output voltage

V_{DIODE}: Output diode forward voltage

f_{OSC}: Switching frequency, Hertz

The inductor current ripple is typically set for 20% to 40% of the maximum inductor current. High frequency ferrite core inductor materials reduce frequency dependent power looses compared to cheaper powered iron types, improving efficiency. The inductor should have low DCR (series resistance of the winding) to reduce the I^2R power losses, and must not saturate at peak inductor current levels.

Capacitor Selection

The internal loop compensation of the ST3710 boost converter is designed to be stable with output capacitor values of 10μF or greater. Low ESR (equivalent series resistance) capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints. A 10μF to 22μF output capacitor is sufficient for most fixed frequency applications. For applications where Burst Mode operation is enabled, a minimum value of 22μF is recommended. Larger values may be used to obtain very low output ripple and improve transient response. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges. Y5V types should not be used. Case sizes smaller than 0805 are not recommended due to their increased DC bias effect.

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from battery, If follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 22μF input capacitor connected to inductor is sufficient for most applications. Larger values maybe used without limitations. For applications where the power source is more than a few inches away, a larger bulk decoupling capacitor is recommended on the input to the boost converter.

Diode Selection

A Schottky diode should be used for the output diode. The forward current rating of the diode should be higher than the load current, and the reverse voltage rating must be higher than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

PCB Layout Consideration

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

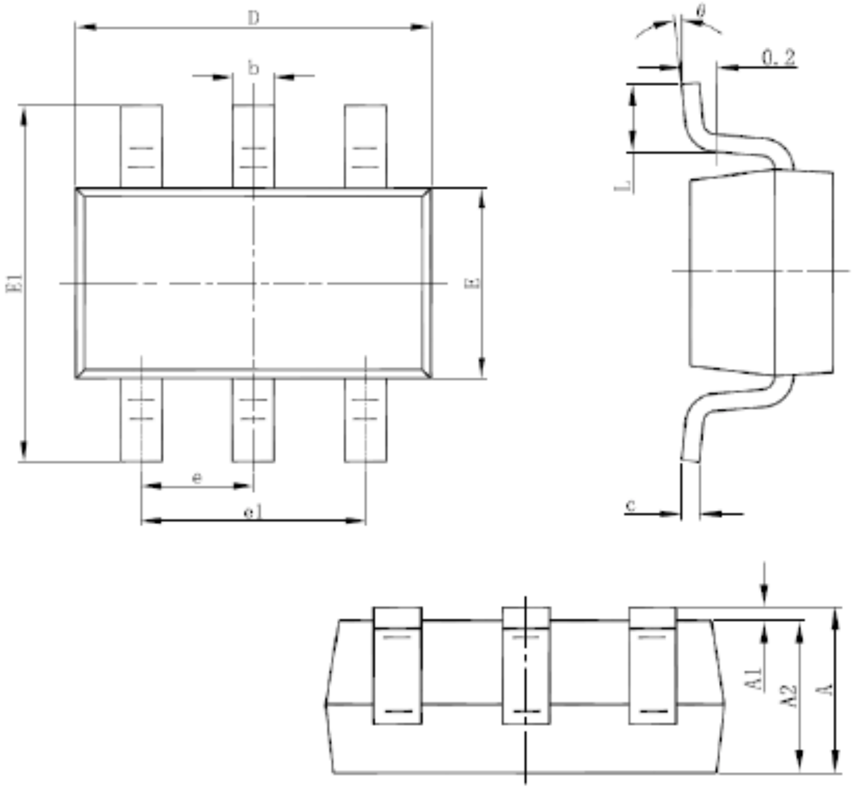
1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the C_{IN} input capacitor, to the regulator IN terminal, to the regulator LX terminal, to the inductor then out to the output capacitor C_{OUT} and load. The second loop starts from the output capacitor ground, to the regulator GND terminals, to the inductor and then out to C_{OUT} and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the IN terminal. Grounding for both the input and output capacitors should consist of a small localized topside plane that connects to GND. The inductor should be placed as close as possible to the LX pin and output capacitor.
2. Minimize the copper area of the switch node. The LX terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the LX terminal. The inductors should be placed as close as possible to the LX terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback

components should be connected together then route to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.

4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the LX pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

PACKAGE DIMENSION

SOT-23-6L



SYMBOL	Dimensions in Millimeters		Dimensions in Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°